

## CLAIMS

What is claimed is:

- 1 1. A computer system comprising:  
2 a backplane that includes:  
3 multiple sockets;  
4 a bus that couples the multiple sockets together,  
5 wherein the bus includes a capability signal line; and  
6 a circuit board inserted in one of the multiple sockets, and configured to limit a voltage  
7 on the capability signal line to one of three or more predetermined values, wherein the  
8 predetermined values are indicative of different bus component capability levels.
- 1 2. The system of claim 1, wherein the predetermined values are indicative of a maximum bus  
2 clock rate supported by the circuit board.
- 1 3. The system of claim 1, wherein the circuit board includes a voting circuit that limits the  
2 voltage on the capability signal line when the voting circuit is enabled.
- 1 4. The system of claim 3, wherein the voting circuit includes a zener device configured to limit  
2 the voltage to less than a predetermined value that is indicative of the capability level of the  
3 circuit board.
- 1 5. The system of claim 3, wherein the circuit board further includes a sample circuit that latches  
2 a digital value indicative of the voltage on the capability signal line.

1 6. The system of claim 5, wherein the circuit board further includes a hold circuit coupled to the  
2 sample circuit to receive the digital value and configured to maintain the capability signal line at  
3 a voltage indicated by the digital value when the voting circuit is disabled.

1 7. The system of claim 1, further comprising multiple circuit boards inserted in corresponding  
2 sockets and configured to limit the voltage on the capability signal line to a predetermined value  
3 that is indicative of the capability level of the corresponding circuit board, whereby the voltage  
4 on the capability signal line is determined by the circuit board having the lowest voltage limit.

1 8. The system of claim 1, wherein the backplane further includes a circuit to power the capability  
2 signal line at a voltage no higher than a predetermined voltage that is indicative of the capability  
3 level of the backplane.

1 9. The system of claim 1, wherein the circuit board includes:  
2 a processor;  
3 a memory coupled to the processor;  
4 a bridge device coupled between the processor and the backplane; and  
5 a long-term storage device coupled to the bridge device.

1 10. A computer system comprising:  
2 a processor;  
3 a memory coupled to the processor;

4 a peripheral bus;  
5 a bridge device coupled between the processor and the peripheral bus; and  
6 a long-term storage device coupled to the bridge device,  
7 wherein the peripheral bus includes a capability signal line having a voltage that is  
8 limited to a predetermined voltage that is one of three or more predetermined voltages each  
9 being indicative of a different capability level.

1 11. The system of claim 10, further comprising:

2 one or more peripheral components coupled to the peripheral bus, wherein each  
3 peripheral component is configured to limit the voltage on the capability signal line to a  
4 corresponding predetermined voltage that is indicative of a corresponding capability level of the  
5 peripheral component.

1 12. The system of claim 11, wherein the capability level is the maximum bus clock frequency  
2 supported by the peripheral component.

1 13. The system of claim 11, wherein each of the peripheral components includes a voting circuit  
2 having a zener diode configured for a predetermined voltage corresponding to the capability  
3 level of the peripheral component.

1 14. The system of claim 11, wherein each peripheral includes a voting circuit that limits the  
2 voltage on the capability signal line when a peripheral bus reset signal is asserted.

1 15. A method of determining a maximum bus clock rate supported by various components, the  
2 method comprising:  
3 coupling the components to a bus having a capability signal line;  
4 supplying electrical current to the capability signal line, wherein each of the components  
5 limits a voltage on the capability signal line to no more than a predetermined voltage that is  
6 indicative of a maximum bus clock rate supported by the component, each predetermined voltage  
7 being one of a set of three or more predetermined voltages that are indicative of different  
8 maximum clock rates; and  
9 setting a bus clock rate to the maximum clock rate associated with the voltage on the  
10 capability signal line.

1 16. The method of claim 15, further comprising:  
2 asserting a bus reset signal while supplying electrical current to the capability signal line.

1 17. The method of claim 16, further comprising:  
2 measuring the voltage on the capability signal line after asserting the bus reset signal; and  
3 holding the voltage on the capability signal line at the predetermined voltage associated  
4 with the bus clock rate.

1 18. The method of claim 15, wherein the components include zener devices configured in  
2 accordance with the maximum bus clock rate supported by the components.

1 19. The method of claim 18, further comprising:

2 disabling the zener devices when a bus reset signal is de-asserted.

1 20. The method of claim 17, further comprising:

2 detecting a voltage held on the capability signal line while the bus reset signal is de-

3 asserted; and

4 determining if the voltage held on the capability signal line is consistent with a bus

5 capability of a newly added bus component.

1 21. The method of claim 20, further comprising:

2 allowing the newly added bus component to participate in bus transactions if the voltage  
3 held on the capability signal line is consistent with the bus capability of the newly added bus  
4 component.

1 22. The method of claim 20, further comprising:

2 preventing the newly added bus component from participating in bus transactions until  
3 the bus reset signal is next asserted.